Fifty Years of the 555 Timer – A Tribute from a Didactic IC Design Perspective

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***Abstract*—The 555 timer is considered the most popular integrated circuit in the world, and completed fifty years in 2022. It can be used for implementing different temporization schemes. This work describes a class project regarding the design of a conceptual replica of the 555, for a 0.5 μm process. Free tools were used for simulation, design, and verification. The main blocks of the circuit are described, as well as its layout, and simulation results for the extracted circuit are shown.**

***Index Terms*—microelectronics, integrated circuit design, timer, 555 IC, free tools, open source tools.**

I. Introduction

The integrated circuit (IC) called 555 was released in 1972 by Signetics Corporation. This component was designed with the objective of generating timing signals of adjustable duty cycle and frequency for use in electronic applications [1]. The chip was designed to be flexible, which led to it being used in ways outside what the designer had predicted [2]. As such, over the years, it has become one of the most popular and versatile chips in electronics, with a wide range of applications. It generated a great impact in the world of electronics, as it brought simple and effective solutions for timing circuits at a low cost. The 555 has three main operating modes: monostable, bistable, and astable. With these operating modes it can be used as a timer, analog to digital signal converter, frequency divider, flip-flop, and many others [3].

The 555 was initially designed with bipolar junction transistor (BJT) since it was still the dominant technology for analog designs [4]. However, several advances were made in regard to the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) technology, along with usage techniques and production. This led the device to be commercially viable not only for applications that naturally thrived with greater miniaturization but also for general-purpose analog circuits. In fact, some characteristics of the voltage-controlled transistor can prove useful for these designs, such as lower idle power consumption, high input impedance, and lower minimum operating voltage.

With the rise of the MOSFET, complementary MOS (CMOS) 555 designs were eventually made, and versions based on both technologies can be found still in production to date. Comparing two devices from the same manufacturer, one bipolar based (LM555 [5]), and another CMOS-based (LMC555 [6]), the advantages cited in the previous paragraph become apparent: the CMOS 555 draws an idle input current about 100 times lower, works at a third of the minimum voltage, and can operate at higher frequencies. It achieves all these features while costing only about 20% more than the bipolar counterpart.

In this work, as an homage to the history of this IC, ever so present in the learning path of many electronics engineers even today, a full version of the chip was designed [7], with the usage of open-source software, and later simulated in typical application circuits. In Section II, the circuit description is presented, from the basic block diagram. The layout itself is described in Section III, correlating each block with the previous block diagram. In Section IV, the simulation results are shown and discussed. Finally, the conclusions are presented in Section V.

II. Circuit Description

The block diagram of the designed timer is shown in Fig. 1. Its structure is very similar to that encountered in the 555 datasheets of different versions. It is constituted by two comparators, which are, in this case, simply implemented by open-loop, one-stage operational transconductance amplifiers (OTAs). The outputs of the amplifiers are followed by digital buffers, in order to sharpen the response of the amplifiers. Each signal is then connected to the inputs of an R-S latch, which has an extra, active-low Clear input.

The output Q_b of the latch is applied on an output buffer, which has to be capable of driving a load connected at the

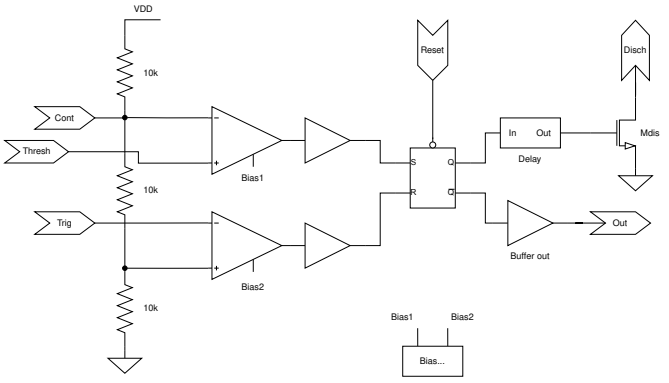

Fig. 1. The 555 block diagram.

output Out, by sourcing and sinking a current in the order of several miliampères.

The output Q of the latch drives the discharge transistor, which has a large aspect ratio, in order to also promote the discharge of an external capacitor. Between the output Q of the latch and the discharge transistor, M_{dis}, a delay line was placed. Although it is not present in the original 555 block diagrams, the need for a delay in the signal applied to the gate of M_{dis} was verified, particularly for the case of the monostable multivibrator.

At the inputs of the comparators, there is the typical resistor string, composed of three equal resistors. It is curious that the name "555" is associated with three resistors with 5 $k\Omega$ each, although the former designer, Hans Camenzind, stated that the name was arbitrarily chosen [8]. Actually, the only need is that the resistors must have the same value. In this project, three resistors of 10 $k\Omega$ each were chosen.

The resistor string puts a voltage value on the positive input of the lower comparator equal to $\frac{1}{3} \cdot V_{DD}$, where V_{DD} is the supply voltage while putting $\frac{2}{3} \cdot V_{DD}$ in the negative input of the upper comparator, which is also connected to a $Cont$ pin (normally, connected to an external filter capacitor). By controlling the increase and decrease of the signals on Trigger and Threshold, with the aid of the discharge output ($Disch$), it is possible to achieve a unique pulse in Out (monostable operation) or a periodic pulse (astable operation). For a monostable operation, an external pulse is necessary, while for an astable operation, no external stimulus is needed.

The block diagram also shows a biasing circuit, used to bias the two comparators. The main blocks are depicted in the following items.

A. Comparator

The comparator diagram is depicted in Fig. 2. It is a single stage operational transconductance amplifier (OTA), designed for a rated biasing current of 40 μA, with a PMOS differential pair. Dimensions of the transistors (W/L, in $\mu m/\mu m$) and multiplicity M are indicated in the figure. Different from the original design of the 555, the same type of differential pair was used in both the upper and lower comparator. In other words, the comparators here are identical circuits.

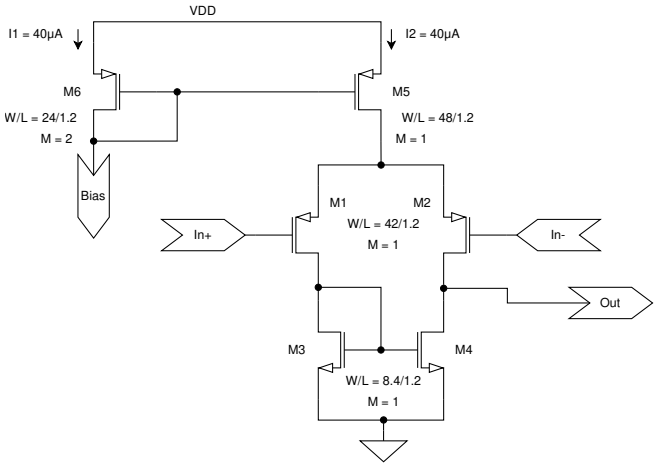

Fig. 2. Comparator (single-stage OTA).

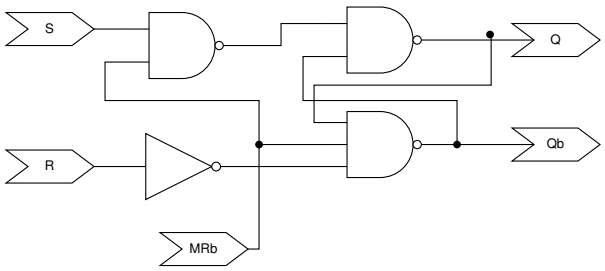

Fig. 3. RS latch.

B. Buffers

The two buffers are constituted by transistors with aspect ratios close to the minimum, simply by connecting two inverters in a cascade.

C. RS latch

The RS latch is composed of an arrangement of two and three-input NAND ports and inverter, as shown in Fig. 3. Note that an active-low Master Reset (MR_b) overwrites any combination of inputs in R and S, forcing the outputs Q and Q_b to 0 and 1, respectively.

D. Output buffer

The output buffer is composed of two cascaded inverters, with transistors with higher aspect ratios, suited for sourcing or sinking currents in the order of magnitude of some miliampères.

E. Discharge transistor

In order to discharge external capacitors with up to several hundreds of microfarads, the discharge transistor must also have a large aspect ratio. For M_{dis} (in Fig. 1), W/L = 24/0.6, M = 8.

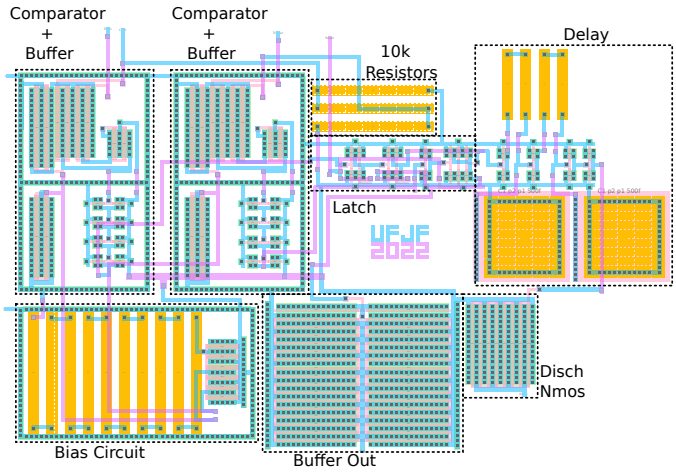

Fig. 4. Circuit layout.

F. Delay line

The delay line is composed of two inverters, each followed by an RC circuit, where R = 10 k and C = 500 fF. The purpose is to cause a time delay of approximately 10 ns between the latch output (Q) and the input of the discharge transistor, M_{dis}.

III. Circuit Layout

The replica of 555 was laid out for the ON Semi 0.5-um standard CMOS process (N-well, three metal, two poly, 5 V supply), by using the scalable CMOS design rules (SCMOS) [9]. Poly-poly capacitors and high-resistive poly resistors were used for the $R-C$ elements of the delay line.

The open-source Electric VLSI Design System [10] was employed for the layout, due to the ease of use for students, and also due to the ability of the software to perform DRC (design rule checking), ERC (electrical rule checking) and LVS (layout versus schematics) tests. In Electric, LVS is named NCC (network consistency checking). SCMOS design rules are native in Electric.

The layout is shown in Fig. 4, with an indication of the main parts. The total area of the circuit was close to 0.025 mm^2. The .jelib file containing the layout can be found in [7].

IV. Simulation Results

The layout described in previous sections was extracted for post-layout simulation in LTSpice XVII, by employing the 0.5 μm MOSFET models available in [11]. Although the 555 timer allows a variety of circuit implementations, in this work, for simplicity, the results for two typical configurations are shown: astable and monostable. The supply current drained by our design was at about 400 µA, which is 4 times larger than that of the commercial CMOS design, and 7.5 times lower than that of the BJT based design.

A. Astable mode of operation

Considering the circuit testbench shown in Fig. 5, and as explained in [6], the astable mode of operation produces fixed-frequency pulses, governed by the equations:

$$t_{on} = 0.693 \cdot (R_A + R_B) \cdot C \tag{1}$$

$$t_{off} = 0.693 \cdot R_B \cdot C \tag{2}$$

Where t_{on} is the charge time (output high interval) and t_{off} is the discharge time (output low interval). The oscillation period, T, is then defined by

$$T = 0.693 \cdot (R_A + 2 \cdot R_B) \cdot C \tag{3}$$

Fig. 6 shows the results for the circuit output using $R_A = 2.7\ k\Omega$, $R_B = 10\ k\Omega$ and $C = 100\ nF$, as well as the voltage across the capacitor, which oscillates between 1/3 and 2/3 of V_{DD}. The obtained frequency for this example was 635 Hz.

The high level value of the output voltage was close to 4.90 V for a load of 1 kΩ, demonstrating the capability of the output buffer on supplying a current close to 5 mA without considerable voltage drop. For a 100-Ω load, a voltage drop close to 0.9 V was achieved (supplying a current close to 40 mA).

To test the frequency limits of the IC, the load was put to a high value (100 $k\Omega$), and the components that change the frequency were lowered until the expected operation failed.

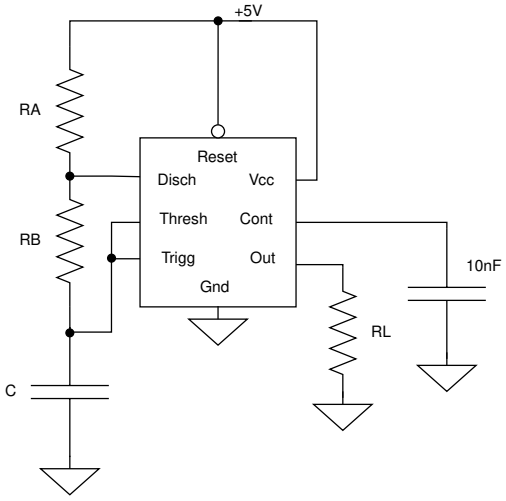

Fig. 5. Astable circuit.

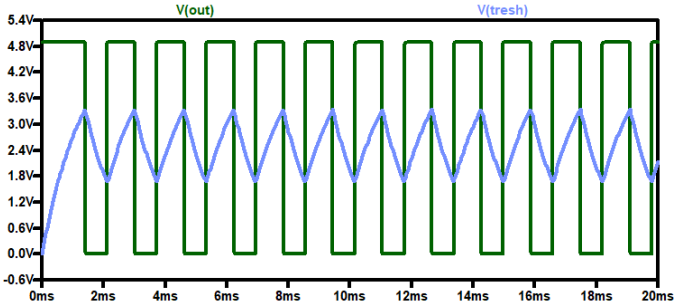

Fig. 6. Astable circuit simulated waveforms. Green: circuit output voltage; Blue: capacitor voltage.

For $R_A = 55\ \Omega$, $R_B = 0\ \Omega$ (short circuit), and $C = 0\ F$ (open circuit), the maximum frequency achievable was 30.4 MHz. The actual frequency could not be calculated with the previous equations, since the intrinsic capacitances and resistances dominated the response.

B. Monostable mode of operation

For the monostable mode, an external, active-low trigger pulse must be applied in the $Trigg$ input, as depicted in Fig. 7, in order to produce a pulse with width t_W. Upon the trigger pulse, the capacitor begins to charge until its voltage reaches 2/3 of V_{DD}. During this charging interval, the output pulse remains at a high level, according to

$$t_W \approx 1.1 \cdot R_D \cdot C \tag{4}$$

As an example, the post-layout simulation was done, by using $R_D = 12\ k\Omega$ and $C = 470\ \mu F$, leading to a pulse with t_W = 6.21 s, as shown in Fig. 7, which shows the generated pulse and the voltage across the capacitor. The minimum pulse obtained was $t_W = 21.51\ \mu s$, using $R_D = 250\ \Omega$ and $C = 390\ nF$.

Both results for the astable and monostable operation did not take into account the effects of pad capacitances. The pads design was beyond the scope of the project and was not included. Moreover, it should be considered that the layout can be employed as a block of another circuit. But simulation tests with capacitances or order of few picofarads at the external pins (the typical capacitances of the pads) did not alter the results, except for the upper limit frequencies (for astable) or the lower limit generated pulses (in case of monostable).

V. Conclusion

This paper presented the design of a circuit intended to be a replica of the well-known 555 timer, which completed fifty years in 2022, with several versions since its first release. The popularity of this IC can be associated with its low cost, simplicity of use, and great availability in the market, which

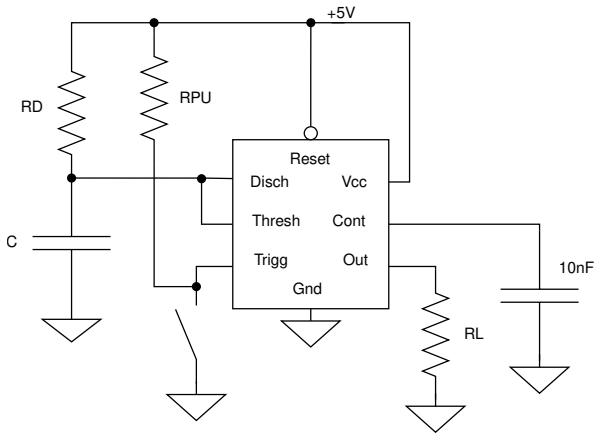

Fig. 7. Monostable circuit.

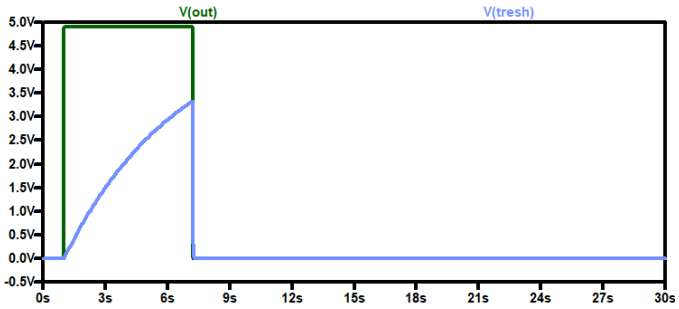

Fig. 8. Monostable circuit simulated waveforms. Green: circuit output voltage; Blue: capacitor voltage.

makes it the timer choice for a huge quantity of professional and amateur electronic projects.

The design of a 555 replica was proposed as a class project, in order to pay tribute to the golden jubilee of this IC. The constructed block can be employed as a subcircuit of more complex IC designs.

A free tool was used for simulation, and an open-source tool for the layout, verification, and extraction. For this project, the team avoided simply copying the original topology, available in the literature and online media, and instead started a new project from its block diagram, encountered in the datasheets.

From the didactic point of view, the design of a 555 replica was a great opportunity to review some concepts, such as the design of comparators, latches, output stages, and the integration of these blocks. Moreover, it contributed to the learning of the methodology of circuit extraction and post-layout simulation with external components.

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